

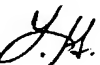





INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>		Docket Number (Optional) SC12042ZK		Application Number Unknown	
		Applicant(s) Wang et al.			
		Filing Date July 31, 2003		Group Art Unit Unknown	
*EXAMINER INITIAL	OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>				
	1	John C. Carson, "Advances in Chip Level Packaging" (2002 Lecture notes, Johns Hopkins University)			
	2	"MicroPro Proves Effective for uBGA Sphere Attach", Speedline (a publication of Speedline Technologies), Issue #2 (Summer 2001)			
	3	D. Light, D. Castillo, M. Beroz, M. Nguyen, and T. Wang, "Vertical Expansion (WAVE) Packaging Process Development" (published by Tessera Technologies, 2001)			
	4	Joseph Fjelstad, "Strategies for Creating Compliant IC Packages at Near Chip Size" (INTERPACK 1999)			
	5	K. Klein, T. Leichle, E. Moss, P. Sassone and X. Wei, "A Survey of Compliant Interconnects for Wafer Level Packaging" (December 13, 2001)			
EXAMINER		DATE CONSIDERED			
		12/10/03			
<small>*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small>					